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(54) HIGH VOLTAGE RESISTANT MOS TRANSISTOR

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SPECIFICATIONS

1. Title of the Invention: High Voltage Resistant MOS Transistor

2. Scope of the Patent's Claims:

1. A high voltage resistant MOS transistor, characterized by the fact that it is equipped with a source and drain region of the second conductive type, formed in the shape of a comb and mutually separated from a semiconductor substrate of the first conductive type,

a low impurity concentration region of the second conductive type formed on the side of said drain region,

as well as a channel region, formed between said low impurity concentration region and said source region,

wherein the channel length of a curved part of the channel region, formed in the front end part of said source region, is longer than said curved part of the drain region.

3. Detailed Explanation of the Invention

This invention relates to a MOS transistor construction with a drain which is highly resistant to voltage.

Because MOS transistors have generally a much higher switching speed when compared to bipolar transistors, they are used mainly as power elements and high-frequency elements having a positive coefficient of input characteristics.

Figure 1 shows a profile view of a common MOS transistor. As shown in Figure 1, (1) indicates a P type silicon substrate, (2) and (3) are N^+ type source and drain regions, respectively, (4) is a gate oxide film, and numbers (5), (6), and (7) indicate a source electrode, a drain electrode, and a gate electrode. In addition, the part shown in Figure 1 by the broken line indicates an equipotential line when a drain voltage is applied. Although the drain voltage is limited by the junction withstand voltage of drain region (3) and substrate (1), one can clearly see from the equipotential line that in reality, the voltage is determined depending on the concentration of the electric current in the vicinity of the surface of drain region (3), which depends on the combined influence of gate electrode (7) and drain region (3). When gate oxide film (4) is approximately 1,000 Å thick, the drain voltage resistance will reach only about 50 V.

Figure 2 is a profile view showing the construction of a MOS transistor characterized by an improved drain voltage resistance. Number (8) is a P type silicon substrate, numbers (9) and (10) indicate an N^+ type source and drain region, respectively, (11), (12), and (13) are a source electrode, a drain electrode, and a gate electrode, respectively, and an N^- type low impurity

concentration region (15) is created in the direction from drain region (10) to channel region (14).

[page 2]

Depending on the formation of this low impurity concentration region (15), the equipotential line can be extended in the direction of channel region (14) as shown by the broken line, which makes it possible to increase the drain resistance voltage from 300 V to 400 V by preventing electric current concentration in the vicinity of the surface of drain region (10). This low impurity concentration region (15) is commonly called a drift channel.

On the other hand, although it is possible to increase the gate width W and to shorten the gate length L based on gm δ W/L in order to obtain a high reciprocal conductance gm (W is the gate width and L is the gate length), since the length of the gate cannot be too short, normally, it is formed in the range of 2 ~ 7 μ. Therefore, it is known that a comb shaped construction can be used for the source and drain region in order to increase the width of the gate. Figure 3 shows a partial surface view of such a MOS transistor. As shown in Figure 3, (16) indicates a P type silicon substrate, (17) and (18) are an N^+ conductive type source region and drain region, respectively, (19) is an N^- conductive type low impurity concentration region and (20) is a channel region. Source region (17) and drain region (18) are combined so as to form together a comb shape. Accordingly, it is possible to increase the gate width because channel region 20 is formed in a zigzag shape.

However, since the lines of electric force are concentrated as shown by the channel marks in the direction toward the front end part of channel area (20) of protruding area (17) from the vicinity of the base of the comb shape of drain area (18), it is not possible to improve the status of the breakdown electric current and breakdown voltage which is caused by a breakdown yield status in the boundary between the low impurity concentration area (19) and the curved part of channel area (20). As shown in Figure 5 which is a graph indicating the yield breakdown, at the point when the drain breakdown voltage V_{DSS} is applied, a yield breakdown will be generated by electric current in the point indicated by point a, and at this time, the electric current will be characterized by a breakdown current $I_{BR(P)}$. In the construction which is shown in Figure 3, the breakdown voltage V_{DSS} is approximately in the range of 300 V ~ 400 V and the breakdown current $I_{BR(P)}$ is approximately in the range of 1 ~ 3 mA.

In view of the above described problems, this invention provides a highly voltage resistant MOS transistor which eliminates the above described disadvantages. The following is a detailed explanation of this invention which is based on the enclosed figures.

Figure 4 shows a partial top view of one embodiment of this invention. In this figure, (21) indicates a P type silicon substrate, (22) and (23) are an N^+ conductive type source and drain region, respectively, (24) is an N^- conductive type low impurity concentration region, and (25) is a channel region.

Layer resistance Rs in the range of approximately 10 ~ 20 Ω is used in P type silicon

substrate 21. Low impurity concentration region (24), which can be formed by epitaxial growth or ion implantation, etc., forms a layer having resistance Rs = 8 Ω cm, with a depth of about 20 μ. On the other hand, source region (22) and drain region (23) are formed by diffusion so that they both create a combined comb shape. Channel region (25) between them is formed with an implanted impurity of the P type created by ion implantation, making it possible to control a specific channel concentration. The channel length of channel region (25) is 3 μ and the channel is formed with a width of 120 nm.

In addition, the front end part of source region (22) is formed with a sufficiently larger corresponding curve R' of channel region (25) than the curve of the curved part in the base of drain region (23), and length l' of the low impurity concentration region (24) from drain region (23) to channel region (25) is longer than length l. Due to this formation, the electric force lines will be created longer from the base of drain region (23) toward the curved part of channel region (25), and the electric field will be weakened in this part, which prevents concentration of electric current.

Figure 6 is a graph showing the results of a case when the lengths R' = 10 μ, 20 μ are used. When R' = 10 μ, the breakdown voltage V_{DSS} will be about 430 V, and the breakdown current $I_{BR(P)}$ will be 8 mA ~ 20 mA. When R' = 20 μ, the breakdown voltage V_{DSS} will be about 450 V and the breakdown current $I_{BR(P)}$ will be about 15 mA ~ 30 mA. Accordingly, as one can see clearly from the results shown in Figure 6, breakdown voltage V_{DSS} can be increased above 400 V and a high voltage resistance design can be achieved while the breakdown current $I_{BR(P)}$ at can be also greatly improved at the same time.

As was explained above, when a sufficiently greater curve ratio of the curved part corresponding to the drain region is used with a corresponding curve ratio of the channel region formed in the front end part of the source region in this invention, the breakdown voltage and the breakdown current can be greatly improved because this makes it possible to prevent concentration of electric current in the boundary between the curved channel region and the low impurity concentration region.

4. Brief Explanation of Figures

Figure 1 shows a partial profile view of an example of prior art, Figure 2 shows a partial profile view of an improved example of prior art, Figure 3 shows a top view of a MOS transistor according to prior art, Figure 4 shows a top view indicating an embodiment of this invention,

[page 3]

Figure 5 is a graph explaining the relationship between breakdown voltage V_{DDS} and breakdown current $I_{BR(P)}$, and Figure 6 is a graph indicating the results of a test of the embodiment shown in Figure 4.

(21) ... P-type silicon substrate, (22) ... source region, (23) ... drain region, (24) ... low impurity concentration region, (25) ... channel region.

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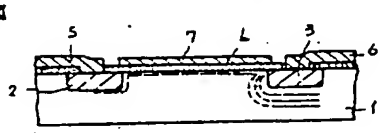
(Figure 1, 2, 3, 4, 5, and 6)

第1図



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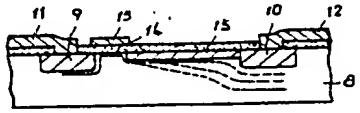
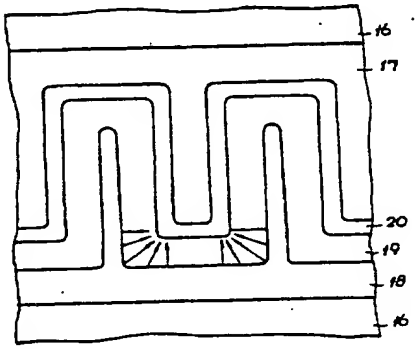
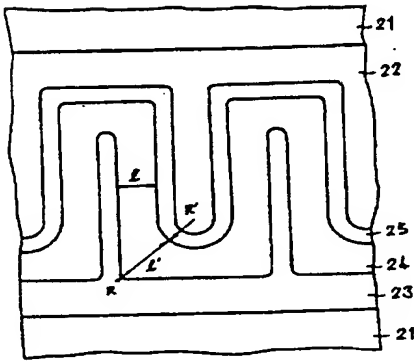


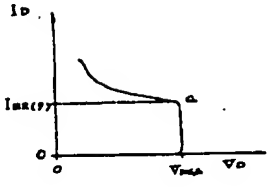
第3図



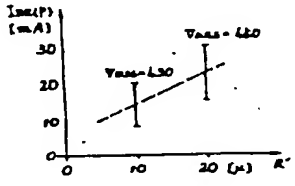
第4図



第5図



第6図



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（全 3 頁）

⑭高耐圧ＭＯＳトランジスタ

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㉒出　　願　昭55(1980) 6 月25日
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明　　細　　書

1. 発明の名称　高耐圧ＭＯＳトランジスタ

2. 特許請求の範囲

1. 第１導電型半導体基体上に互いに離れて櫛形に形成された第２導電型のソース、ドレイン領域と、該ドレイン領域側に形成された第２導電型の低不純物濃度領域と、該低不純物濃度領域と前記ソース領域との間に形成されたチャンネル領域とを備え、前記ソース領域の先端部に形成されたチャンネル領域の曲折部の曲率を対応する前記ドレイン領域の曲率よりも十分大きく形成することを特徴とする高耐圧ＭＯＳトランジスタ。

3. 発明の詳細な説明

本発明はドレイン耐圧の高いＭＯＳトランジスタの構造に関する。

一般にＭＯＳトランジスタはスイッチングスピードがバイポーラトランジスタに比べて非常に早く、入力特性が正の係数を持っている為主に高周波素子及びパワー用素子として用いられる。

通常のＭＯＳトランジスタの断面構造を第１図に示す。第１図に於いて、(1)はＰ型シリコン基板、(2)(3)はそれぞれＮ＋導電型を有するソース、ドレイン領域、(4)はゲート酸化膜、(5)(6)(7)はそれぞれソース電極、ドレイン電極、ゲート電極を示す。また第１図中に示された破線はドレイン電圧を印加した場合の等電位線である。ドレイン耐圧はドレイン領域(3)と基板(1)との接合耐圧で制限されるが、実際には等電位線から明らかな様に、ゲート電極(7)とドレイン領域(3)との重なりに依って生じるドレイン領域(3)表面近傍の電流集中に依って決定され、ゲート酸化膜(4)が１０００Ａ程度の場合にはドレイン耐圧は５０Ｖ程度にしかならない。

第２図はドレイン耐圧を向上させたＭＯＳトランジスタの断面構造であり、(8)はＰ型シリコン基板、(9)(10)はそれぞれＮ＋導電型のソース、ドレイン領域、(11)(12)(13)はそれぞれソース電極、ドレイン電極、ゲート電極であり、ドレイン領域(10)からチャンネル領域(14)方向にＮ⁻型の低不純物濃度領域(15)が設けられている。この低不純物濃度領域(15)を形成することに依り、等電位線は破線で示される

06くチャンネル領域04方向に延在され、ドレイン領域02表面近傍の電流集中が防止されドレイン耐圧は３００Ｖから４００Ｖ程度まで向上する。この低不純物濃度領域05は一般にドリフトチャンネルと呼ばれている。

一方高い相互コンダクタンスｇｍを得るためには$g_m \propto \frac{W}{L}$（Ｗはゲート幅、Ｌはゲート長）よりゲート長Ｌを短かくしゲート幅Ｗを大きくすれば良いが、ゲート長Ｌはあまり極端に短かくすることは出来ず通常２～７μ程度に形成される。そこでゲート幅を大きくするためにソース、ドレイン領域を櫛形に形成する構造が知られている。第３図はＭＯＳトランジスタの一部表面図である。第３図に於いて、08はＰ型シリコン基板、07 09はそれぞれＮ＋導電型のソース、ドレイン領域、09はＮ－導電型の低不純物濃度領域、04はチャンネル領域であり、ソース領域07及びドレイン領域09はそれぞれ櫛形に形成され組合わされている。従ってチャンネル領域04はジグザグに形成されるのでゲート幅を大きくすることができる。しかしドレイン

Ｐ型シリコン基板01には層抵抗ＲＳが１０～２０Ω㎝程度のものが使用され、低不純物濃度領域04はエピタキシャル成長あるいはイオン注入等に依って層抵抗ＲＳ＝８Ω㎝、深さ２０μ程度に形成される。一方ソース領域02及びドレイン領域03は互いに組合わせられた櫛形の形状に拡散に依って形成され、その間のチャンネル領域04はイオン注入に依ってＰ型不純物が注入され、所定のチャンネル濃度となる様制御される。このチャンネル領域04はチャンネル長が３μ、幅が１２０㎜となっている。

またソース領域02の先端部に於いて、チャンネル領域04の曲折部の曲率Ｒ′を対応するドレイン領域03の根元での曲折部の曲率Ｒより十分大きく形成し、ドレイン領域03からチャンネル領域04までの低不純物濃度領域04の長さℓ′を他の区分の長さℓより長くする。この様に形成することに依り、ドレイン領域03の根元からチャンネル領域04の曲折部に向う電気力線が長くなりこの部分での電界が弱まり、電流集中が防止される。

イン　域08の櫛形の根元付近からソース領域07突出した先端部のチャンネル領域04に向かって印で示される如く電気力線が集中し、チャンネル領域04の曲折部と低不純物濃度領域09での境界破壊を生じ、降伏降伏電圧及び降伏電流を向上することができなった。降伏破壊は第５図に示すグラフに於いて、ドレインに降伏電圧ＶＤＳＳを印加した時、Ｂで示される電流で降伏破壊を生じ、この時の電流が降伏電流ＩＢＲ(P)である。第３図に示される構造では降伏電圧ＶＤＳＳは３００Ｖ～４００Ｖ程度であり、降伏電流ＩＢＲ(P)は１～３ｍＡ程度であった。

本発明は上述した点に鑑みて為されたものであり、従来の欠点を除去した高耐圧ＭＯＳトランジスタを提供するものである。以下図面を参照して本発明を詳細に説明する。

第４図は本発明の実施例を示す一部表面図であり、01はＰ型シリコン基板、02 03はそれぞれＮ＋導電型のソース、ドレイン領域、09はＮ－導電型の低不純物濃度領域、04はチャンネル領域である

第６図は曲率Ｒ′＝１０μ、２０μとした場合の実験結果である。Ｒ′＝１０μの場合には降伏電圧ＶＤＳＳは４３０Ｖ程度、降伏電流ＩＢＲ(P)は８ｍＡ～２０ｍＡ、Ｒ′＝２０μの場合には降伏電圧ＶＤＳＳは４５０Ｖ程度、降伏電流ＩＢＲ(P)は１５ｍＡ～３０ｍＡになる。従って第６図の結果からも明らかな如く、降伏電圧ＶＤＳＳは共に４００Ｖ以上となり高耐圧化されると共に、降伏電流ＩＢＲ(P)も大幅に向上している。

上述の如く本発明に依ればソース領域の先端部に形成されたチャンネル領域の曲折部の曲率を対応するドレイン領域の対応する曲折部の曲率より十分に大きくすることに依り、曲折したチャンネル領域と低不純物濃度領域との境界に電流集中するのが防止され降伏電圧及び降伏電流が大幅に向上されるものである。

4.　図面の簡単な説明

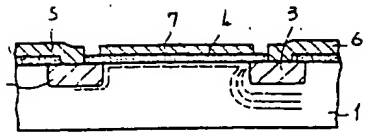
第１図は従来例を示す一部断面図、第２図は従来例の改良された一部断面図、第３図は従来のＭＯＳトランジスタの表面図、第４図は本発明の実

施例を示す表面図、第5図は降伏電圧V_{DSS}と降伏電流$I_{BR(P)}$の関係を示すグラフ、第6図は第4図に示した実施例の実験結果を示すグラフである。

20……P型シリコン基板、22……ソース領域、23……ドレイン領域、24……低不純物濃度領域、25……チャンネル領域。

出願人　三洋電機株式会社　外1名
代理人　弁理士　佐野静夫

第1図



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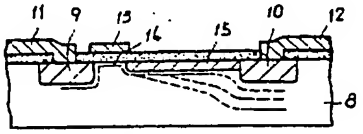

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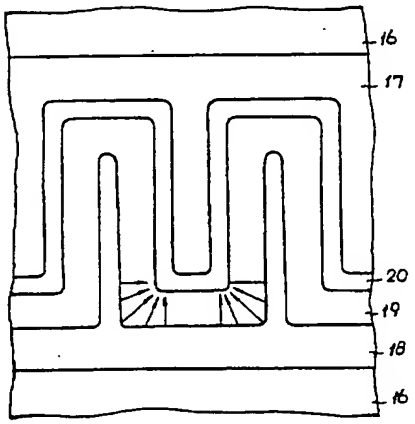

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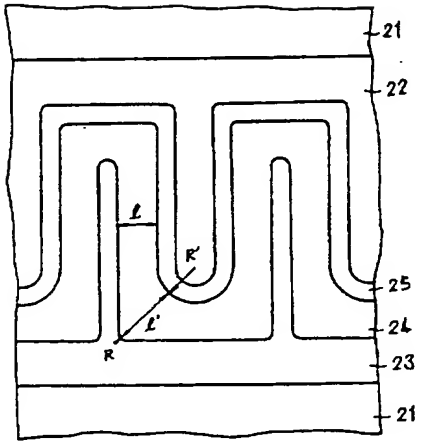
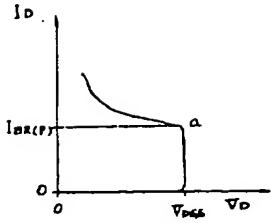


第5図



第6図